IN THE TITLE:

Please replace the title with the following replacement title.

A PROCESSOR CONTROL APPARATUS SWITCHABLY CONTROLLING AND DRIVING ARITHMETIC UNITS, PROCESSOR AND METHOD THEREOF

IN THE SPECIFICATION:

The specification as amended below with replacement paragraphs shows added text with underlining and deleted text with ~~strikethrough~~.

Please REPLACE the paragraph on page 21, starting at line 4:

FIG. 9 shows a block diagram showing an example of a processor comprising two arithmetic units 13c, 14c and ~~two~~ a first instruction control ~~units~~ unit 10c including a first instruction memory 30c and a first instruction decoder 31c and a second instruction control unit 11c. In addition to the configuration of the above-mentioned embodiment 1, the second instruction control unit 11c comprises an instruction queue 35 for temporarily storing series of instructions, an interrupt determination unit 36 for determining whether ~~or not~~ an interrupt can be performed during the execution of a series of instructions, and an AND circuit 37 for obtaining a logical product of the control signal output from the second instruction decoder 33c and the control signal output from the interrupt determination unit 36. The selector 34c switches depending on the output of the AND circuit 37 so that an interrupt can be performed from the first instruction control unit 10c during the independent execution process of the second arithmetic unit 14c. As also shown in FIG. 9, the first instruction control FIG. 10 shows an example of a program containing a plurality of instructions stored in the first instruction memory 30c and the second instruction memory 32c of the processor shown in FIG. 9.

Please REPLACE the paragraph on page 25, starting at line 10 with the following paragraph:

FIG. 13 is a block diagram showing an example of a processor comprising a primary instruction control unit (a 0-th instruction control unit 50 according to the present embodiment), a plurality of secondary instruction control units (the first instruction control unit 10e to the N-th instruction control unit 12e), and a plurality of arithmetic units (the first arithmetic unit 13e to the N-th arithmetic unit 15e) corresponding to the secondary instruction control units. In addition, the first instruction control unit 10e includes a first instruction memory 30e, a selector 34e and a first instruction decoder 31e. The present embodiment has a configuration in which a VLIW type series of instructions 51 is issued from the 0-th instruction control unit 50 to each secondary instruction control unit, and the arithmetic units are synchronously driven as shown in FIG. 13.